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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,405	04/14/2000	Eiji IO	APM-01301	8514

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,405	IO, EIJI	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7,11 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7,11 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. (5,545,575).

Cheng et al. teach in figure 15 a semiconductor device comprising:

(a) a semiconductor substrate 11;

(b) an insulating film 19 formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode 28 formed on said semiconductor substrate, said gate electrode and said insulating film defining at least one lightly doped first drain and source diffusion layer 77', 78';

(d) at least one sidewall 66 covering said gate electrode therewith; and

(e) at least one heavily doped second drain and source diffusion layer 82, 84 formed at a surface of said semiconductor substrate around said gate electrode,

said at least one sidewall having connected thereto a sidewall offset extending outwardly of said gate electrode along the surface of said semiconductor substrate in at least one of regions below which said at least one heavily doped second drain and

source diffusion layer is to be formed, said sidewall offset having a lateral dimension extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a thickness of said sidewall,

(f) low resistive wiring layers 64 formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset,

said at least one heavily doped second drain and source diffusion laver extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said surface of said semiconductor substrate,

wherein said at least one heavily doped second drain and source diffusion layer has an outer lateral dimension along a surface of said semiconductor substrate in a vertical directions and said sidewall offset is formed to have an outer edge which is at approximately said outer lateral dimension of said at least one heavily doped second drain and source diffusion layer.

Cheng et al. do not teach in the embodiment of figure 15 at least one lightly doped first drain and source diffusion layers surrounding at least one heavily doped second drain and source diffusion layers on at least a bottom and a lateral side and extending towards the gate electrode beyond an edge of the sidewall offset.

Cheng et al. teach in the embodiment of figure 7 first drain and source diffusion layers 43, 44 surrounding second drain and source diffusion layers 57, 58 on at least a bottom and a lateral side, wherein the first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides wherein the first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset, in Cheng et al.'s device, in order to improve the device characteristics by forming LDD regions in the device, and in order adjust and optimize the device characteristics by extending the first drain and source diffusion layers towards the gate electrode beyond an edge of the sidewall offset.

Claims 5, 7, 11, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Kunishima et al.

Regarding claim 7, Cheng et al. teach substantially the entire claimed structure, as applied to claims 1 and 6 above, except a silicide layer comprising titanium silicide. Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Cheng et al.'s device, because titanium silicide is a conventional silicide material, of which official notice may be taken.

Regarding claims 5 and 11, Chen et al. do not teach the semiconductor device comprising a memory device. Kunishima et al. teach using the semiconductor device as a CMOS device, and it is well known in the art that CMOS devices are used as memory devices. It would have been obvious to a person of ordinary skill in the art at the time

the invention was made to use Cheng et al.'s device as a memory device, in order to use the device in an application which requires memory device.

Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claims 21 and 23, Kunishima et al. teach in figure 5C a sidewall entirely covering the gate electrode. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

Claims 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Gonzalez (5,439,835)

Cheng et al. teach substantially the entire claimed structure, as applied to claims 1 and 6 above, except a sidewall offset extending in only one direction towards the source and drain diffusion layers.

Gonzalez teaches in figure 9 a sidewall offset extending in only one direction towards the source and drain diffusion layers.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a sidewall offset extending in only one direction towards the source and drain diffusion layers in Cheng et al.'s device, in order to improve the characteristics of the device.

Response to Arguments

Applicant argues that Cheng et al. do not teach that said at least one heavily doped second drain and source diffusion layer has an outer lateral dimension along a surface of said semiconductor substrate in a vertical directions and said sidewall offset is formed to have an outer edge which is at approximately said outer lateral dimension of said at least one heavily doped second drain and source diffusion layer, as recited in claims 1 and 6, because sidewall 66 in figure 15 extending further along the substrate surface than the portions 57 and 58.

Sidewall 66 in figure 15 terminates and has an outer edge at layer 67 or 73. Therefore, Cheng et al. teach that said at least one heavily doped second drain and source diffusion layer has an outer lateral dimension along a surface of said semiconductor substrate in a vertical directions and said sidewall offset is formed to have an outer edge which is at approximately said outer lateral dimension of said at least one heavily doped second drain and source diffusion layer, as recited in claims 1 and 6.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
5/25/06

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